CLAIMS:

The following is a listing of all claims in the application with their status and the text of all active claims:

1.-9. (CANCELED)

10.-15. (CANCELED)

16. (PREVIOUSLY PRESENTED) A content comparing memory device for generating the carry bit or bits in the summation of a search binary word to at least one stored binary word, comprising a plurality of content comparing memory cells arranged in rows and columns, with each stored binary word stored in each of said rows, each of said content comparing memory cells comprising:

(a) a normal memory cell for storing the stored binary bit,

(b) means for reading from and writing to said normal memory cell,

(c) a signal line for delivering the search binary bit,

(d) a first logic device which provides a carry transfer logical operation selected from the group consisting of logical XOR and logical OR of said search binary bit or its inverse and said stored binary bit or its inverse,

(e) a second logic device which provides logical AND of said search binary bit or its inverse and said stored binary bit or its inverse,

(f) an input port for delivering the carry-in value for the bit summation,

(g) an output port for delivering the carry-out value of the bit summation,

(h) said input port connecting to the output port of the previous content comparing memory cell in the row and said output port connecting to the input port of the next content comparing memory cell in the row,

(i) said first logic device driving a passgate between said input port and said output port, said passgate transferring the carry-in value to said output port when turned on,

(j) said second logic device driving said output port to a predetermined carry logical value indicating carry bit in the summation of said stored binary bit or its inverse and said stored binary bit or its inverse,

whereby, the output port of the last content comparing memory cell in a row is driven to the said carry logical value if the summation of the stored binary word of said row, said search binary word, and the carry-in value applied to the input port of the first content comparing memory cell in said row generates a carry.

17. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 16, wherein said normal memory cell stores both said stored bit and its logical inverse.

18. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 16, further including an inverter for creating the logical inverse of said stored bit in each of said content comparing memory cells.

19. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 16, further including a signal line for delivering the inverse of said search binary bit in each of said content comparing memory cells.

20. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 19, wherein said normal memory cell stores both said stored bit and its logical inverse.

21. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 19, further including an inverter for creating the logical inverse of said stored bit in each of said content comparing memory cells.

22. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 16 wherein said first logic device and said second logic device are made from transmission gates,

whereby, the device area becomes smaller.

23. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 22, wherein said normal memory cell stores both said stored bit and its logical inverse.

24. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 22, further including an inverter for creating the logical inverse of said stored bit in each of said content comparing memory cells.

25. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 22, further including a signal line for delivering the inverse of said search binary bit in each of said content comparing memory cells.

26. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 25, wherein said normal memory cell stores both said stored bit and its logical inverse.

27. (PREVIOUSLY PRESENTED) Content comparing memory device of claim 25, further including an inverter for creating the logical inverse of said stored bit in each of said content comparing memory cells.

28.-31. (CANCELED)

32. (PREVIOUSLY PRESENTED) A method for comparing a search binary word to a stored binary word, comprising:

(a) providing a content comparing memory array of same length as said stored binary word which generates, at its output, the carry-out bit for the summation of a binary word applied to it, the binary word stored in the array, and a carry-in value applied at its input,

(b) setting a logical carry-in value of 0 at said input of said content comparing memory,

(c) selecting from the group consisting of:

storing the 2's complement of said stored binary word in said content comparing memory array,

and,

applying the 2's complement of said search binary word to said content comparing memory array,

(d) observing the fact that when a number x is added to the 2's complement of a number y, said carry-out bit will be 1 if $x>y$ and it will be 0 if $x<y$,

whereby, from said output of said content comparing memory it can be judged whether said search binary word is larger than said stored binary word or not.

33. (PREVIOUSLY PRESENTED) A method for comparing a search binary word to a stored binary word, comprising:

(a) providing a content comparing memory array of same length as said stored binary word which generates, at its output, the carry-out bit for the summation of a binary word applied to it, the binary word stored in the array, and a carry-in value applied at its input,

(b) setting a logical carry-in value of 1 at said input of said content comparing memory,

(c) selecting from the group consisting of:

storing the bitwise inversion of said stored binary word in said content comparing memory array,

and,

applying the bitwise inversion of said search binary word to said content comparing memory array,

(d) observing the fact that when binary number 1 is added to the summation of a number x and the bitwise inversion of a number y, said carry-out bit will be 1 if $x>y$ and it will be 0 if $x<y$,

whereby, from said output of said content comparing memory it can be judged whether said search binary word is larger than said stored binary word or not.

34. (PREVIOUSLY PRESENTED) A method for comparing a search binary word to a stored binary word, comprising:

(a) providing a content comparing memory array of same length as said stored binary word which generates an output selected from the group consisting of:

the carry-out bit for the summation of a binary word applied to it, the bitwise inversion of the binary word stored in the array, and a carry-in value applied at its input,

and,

the carry-out bit for the summation of the bitwise inversion of a binary word applied to it, the binary word stored in the array, and a carry-in value applied at its input,

(b) setting a logical carry-in value of 1 at said input of said content comparing memory,

(c) storing said stored binary word as it is in said content comparing memory array,

(d) observing the fact that when binary number 1 is added to the summation of a number x and the bitwise inversion of a number y, said carry-out bit will be 1 if $x>y$ and it will be 0 if $x<y$,

whereby, from said output of said content comparing memory it can be judged whether said search binary word is larger than said stored binary word or not.